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Title:

**PROGRAMMABLE CONDUCTOR RANDOM ACCESS MEMORY AND  
METHOD FOR SENSING SAME**

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TITLE OF INVENTION  
**PROGRAMMABLE CONDUCTOR RANDOM ACCESS MEMORY AND  
METHOD FOR SENSING SAME**

BACKGROUND OF THE INVENTION

1. Field of the Invention:

[0001] The present invention relates to integrated memory circuits. More specifically, it relates to a method for sensing the content of a programmable conductor random access memory (PCRAM) cell.

2. Description of Prior Art:

[0002] DRAM integrated circuit arrays have existed for more than thirty years and their dramatic increase in storage capacity has been achieved through advances in semiconductor fabrication technology and circuit design technology. The tremendous advances in these two technologies have also achieved higher and higher levels of integration that permit dramatic reductions in memory array size and cost, as well as increased process yield.

[0003] A DRAM memory cell typically comprises, as basic components, an access transistor (switch) and a capacitor for storing a binary data bit in the form of a charge. Typically, a charge of one polarity is stored on the capacitor to represent a logic HIGH (e.g., binary "1"), and a stored charge of the opposite polarity represents a logic LOW (e.g., binary "0"). The basic drawback of a DRAM is that the charge on the capacitor

eventually leaks away and therefore provisions must be made to “refresh” the capacitor charge or else the data bit stored by the memory cell is lost.

[0004] The memory cell of a conventional SRAM, on the other hand, comprises, as basic components, an access transistor or transistors and a memory element in the form of two or more integrated circuit devices interconnected to function as a bistable latch. An example of such a bistable latch is cross-coupled inverters. Bistable latches do not need to be “refreshed,” as in the case of DRAM memory cells, and will reliably store a data bit indefinitely as long as they continue to receive supply voltage.

[0005] Efforts continue to identify other forms of non-volatile or semi-volatile memory elements. Recent studies have focused on resistive materials that can be programmed to exhibit either high or low stable ohmic states. A programmable resistance element of such material could be programmed (set) to a high resistive state to store, for example, a binary “1” data bit or programmed to a low resistive state to store a binary “0” data bit. The stored data bit could then be retrieved by detecting the magnitude of a readout current switched through the resistive memory element by an access device, thus indicating the stable resistance state it had previously been programmed to.

[0006] Recently programmable conductor memory elements have been devised. For example, chalcogenide glasses which have switchable resistive states have been investigated as data storage memory cells for use in memory devices, such as DRAM memory devices. U.S. Patents 5,761,115, 5,896,312, 5,914,893, and 6,084,796 all describe this technology and are incorporated herein by reference. One characteristic of a programmable conductor memory element such as one formed of the chalcogenide glasses described above is that it typically includes chalcogenide glass which can be doped with metal ions and a cathode and anode spaced apart on one or more surfaces of the glass. The doped glass has a normal and stable high resistance state. Application of a voltage across the cathode and anode causes a stable low resistance path to occur in the glass. Thus, stable low and high resistance states can be used to store binary data.

[0007] A programmable conductor memory element formed of a doped chalcogenide glass material typically has a stable high resistance state which may be programmed to a low resistance state by applying a voltage across the memory element. To restore the memory cell to a high resistive state, typically one needs to program the cell with a negative, or inverse voltage which is equal to or greater than the voltage used to program the memory element to the low resistance state. One particularly promising programmable conductor chalcogenide glass has a Ge:Se glass composition and is doped with silver.

[0008] Suitable circuitry for reading data from an array of programmable conductor memory elements has not yet been fully developed. Accordingly, in order to realize a functional programmable conductor memory, appropriate read circuitry is required to nondestructively sense data stored in the memory elements of the array.

### SUMMARY OF THE INVENTION

[0009] The present invention provides a sense circuit and method for reading a resistance level of a programmable conductor memory element. In an exemplary embodiment, each programmable conductor memory cell contains a programmable conductor memory element and is coupled between a column line and a word line through a pair of reversely connected diodes, also referred to as an isolation diode pair. In operation, all rows and columns in a given memory array are initially held to the same potential (e.g., a diode threshold voltage plus an additional predetermined voltage). A desired row line connected to a cell to be selected is enabled by bringing it to approximately ground. The difference in voltage potential across the isolation diode pair of a selected cell activates the diodes and initiates current flow through the desired programmable conductor element. A column line associated with the selected cell is then discharged from a precharge value through the diodes and programmable conductor

memory element. The discharging voltage at the column line is compared with a reference voltage a predetermined time after the row line is brought to approximately ground. If the voltage at the column line is greater than the reference voltage, then a high resistance level is recognized, and, if the column line voltage is less than the reference voltage, a low resistance level is detected. The high and low resistance states represent binary data values, i.e., the logical state of the memory element.

[0010] In an alternative embodiment of the invention, a single zener diode can be used in place of the isolation diode pair.

[0011] Once the logical state of the programmable conductor element is read, a refresh operation may optionally be conducted on a memory element programmed to a low resistance state by placing voltage sufficient for programming across the memory element by either increasing the row line voltage or by raising the column line voltage. The programmable conductor element is then re-programmed to its existing logical state and all rows and columns are then returned to their initial operating state for the next operation.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The foregoing and other advantages and features of the invention will become more apparent from the detailed description of preferred embodiments of the invention given below with reference to the accompanying drawings in which:

[0013] Fig. 1 depicts a memory array employing a plurality of PCRAM memory cells, in accordance with an exemplary embodiment of the invention;

[0014] Fig. 2(a) depicts a PCRAM memory cell of Fig. 1 in an isolated state, in accordance with an exemplary embodiment of the invention;

[0015] Fig. 2(b) depicts a PCRAM memory cell of Fig. 1 in a selected state, in accordance with an exemplary embodiment of the invention;

[0016] Fig. 3(a) depicts an alternative PCRAM memory cell in an isolated state, in accordance with an exemplary embodiment of the invention;

[0017] Fig. 3(b) depicts an alternative PCRAM memory cell in a selected state, in accordance with an exemplary embodiment of the invention;

[0018] Fig. 4 depicts a voltage vs. current curve for the PCRAM cell of Figs. 2(a) and 2(b), in accordance with an exemplary embodiment of the invention;

[0019] Fig. 5 depicts a voltage vs. current curve for the PCRAM cell of Figs. 2(a) and 2(b), in accordance with an exemplary embodiment of the invention;

[0020] Fig. 6 depicts a flowchart providing a process flow of a read operation in accordance with an exemplary embodiment of the present invention;

[0021] Fig. 7 depicts an N-sense amplifier of the Fig. 1 memory array, in accordance with an exemplary embodiment of the invention;

[0022] Fig. 8 depicts a P-sense amplifier of the Fig. 1 memory array, in accordance with an exemplary embodiment of the invention;

[0023] Fig. 9 depicts a timing diagram for reading a high resistance level at a programmable conductor element, in accordance with an exemplary embodiment of the invention;

[0024] Fig. 10 depicts a timing diagram for reading a low resistance level at a programmable conductor element, in accordance with an exemplary embodiment of the invention; and

[0025] Fig. 11 depicts a block diagram of a processor-based system containing a PCRAM memory array, in accordance with an exemplary embodiment of the invention.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0026] The present invention will be described as set forth in exemplary embodiments described below in connection with Figs. 1-11. Other embodiments may be realized and other changes may be made to the disclosed embodiments without departing from the spirit or scope of the present invention.

[0027] Fig. 1 depicts a memory array 100 containing a plurality of PCRAM memory cells (e.g., 108). Memory array 100 also includes a plurality of column (bit) lines (e.g., 104), row lines (e.g., 106) and sense amplifiers (e.g., 102). Also depicted in memory array 100 is a first precharge circuit 116 for precharging all row lines to a common initial voltage (e.g., a diode threshold voltage  $V_t$  plus a predetermined voltage  $V$  (e.g., 0.2v)) and a second precharge circuit 118 for precharging all column lines to the same predetermined voltage as the row lines (e.g.,  $V_t+V$ ). For reasons of simplicity, only two row lines and two column lines are depicted as being respectively coupled to the precharge circuits 116, 118. Precharge circuit 116 contains a first transistor 177 and a second transistor 179. A first source/drain terminal of transistor 177 is coupled to a first source/drain terminal of transistor 179. A gate terminal of transistor 177 is coupled to a gate terminal of transistor 179 and also to a voltage source for providing the precharge voltage ( $V_t+V$ ). The second source/drain terminals of transistors 177, 179 are respectively coupled to row lines 106, 107. When the precharge signal is received by the precharge circuit 116, all rows are precharged to the predetermined voltage (e.g.,  $V_t+V$ ).

[0028] Similarly, with respect to the second precharge circuit 118, a first source/drain terminal of transistor 181 is coupled to a first source/drain terminal of transistor 183. A gate terminal of transistor 181 is coupled to a gate terminal of transistor 183 and also to a voltage source for providing the precharge voltage ( $V_t+V$ ). The second source/drain terminals of transistors 181, 183 are respectively coupled to column lines 104, 195. Both precharge circuits 116 and 118 may also contain equilibrate circuits, which are not shown for purposes of simplicity.

[0029] Each memory cell 108 contains a programmable conductor memory element 114, a first terminal of which is coupled to column line 104. A second terminal of programmable conductor memory element 114 is coupled to one side of a pair of reverse connected diodes 110, 112 which form an isolation diode pair. The isolation diode pair 110, 112 is also coupled at the other side to row line 106. Each sense amplifier contains two inputs: a first input is received from an associated column line 104 and a second input is received from a Vref line 194 coupled to Vref precharge circuit 192 for precharging the Vref line 194 to Vref when a read operation is initiated. Alternatively, the Vref line 194 may be coupled to precharge circuit 116 and then modified from  $V_t + V$  to Vref (e.g., decreased from  $V_t + 0.2V$  to a lower value such as  $V_t + 0.1V$ ) with a voltage adjusting circuit as known in the art.

[0030] Turning to Fig. 2(a), a simplified schematic diagram of the memory cell 108 is depicted. Memory cell 108 is associated with column line 104 and row line 106. One terminal of the programmable conductor memory element 114 is coupled to column line 104. Another terminal of programmable conductor memory element 114 is coupled to an input of diode 110 and an output of diode 112. An output of diode 110 is coupled to an input of diode 112 and also coupled to row line 106. In accordance with an exemplary embodiment of the invention, to initialize a read operation, both column line 104 and row line 106 are held to the same voltage (e.g.,  $V_t + V$ ). In fact, in an initial state of the memory array 100 prior to a read operation, all row lines and all column lines are held to the same voltage (e.g.,  $V_t + V$ ), thereby preventing any current flow in any memory cell.

[0031] Turning to Fig. 2(b), voltages applied during a read operation of memory cell 108 are depicted. For the read operation the column line 104 of memory cell 108 remains at the initial predetermined voltage (e.g.,  $V_t + V$ ), however, a selected row line is brought to approximately zero volts (e.g., ground). Bringing row line 106 to approximately zero volts creates a voltage potential difference across the memory cell 108. As a result of the voltage potential difference across memory cell 108, diode 110 begins to conduct and current flows from column line 104 to row line 106 through the

programmable conductor memory element 114. When current begins to flow from column line 104 to row line 106, the voltage at column line 104 begins to discharge and there is a voltage drop of  $V_t$  (e.g., 0.3 volts) across the diode pair 110, 112. Assuming that  $V =$  approximately 0.2v, a voltage potential of approximately 0.2 volts remains across the programmable conductor memory element 114. A voltage of approximately 0.2v is sufficient to read the resistance of the programmable conductor memory element 114, but insufficient to program or change a resistance state of the memory element 114.

[0032] The initial voltage to which the column line (e.g., 104) and row line (e.g., 106) are precharged ( $V_t + V$ ) is selected so that when the row line is brought to approximately zero volts the voltage remaining across the programmable conductor memory element 114 is sufficiently high enough to read the contents of programmable conductor memory element 114, but insufficient to program the programmable conductor memory element 114. It should be readily apparent that although specific voltages are described above in connection with the read operation, other voltage combinations may be used as long as a read voltage is applied across the memory element 114 which is sufficient to read the element, but insufficient to program it to a particular resistance state.

[0033] Turning to Fig. 3(a), an alternative embodiment for the PCRAM cell 108 is depicted. PCRAM cell 305 is identical to PCRAM cell 108; however, PCRAM cell 305 contains a single zener diode 300 rather than a reverse connected diode pair 110, 112. Using a single zener diode 300 has some inherent advantages over a reverse connected diode pair 110, 112 including the fact that a memory cell containing a zener diode 300 has a less complex construction. In addition, since the zener diode's 300 breakdown voltage is much greater than that of a conventional diode, it provides greater stability over a wider voltage range. The greater stability means the diode is less susceptible to being activated by system noise or similar interference.

[0034] As shown in Fig. 4, that range of stability for the reverse connected diode pair 110, 112 is approximately 0.6 volts (i.e., from -0.3v to +0.3v). However, as further

shown in Fig. 5, the range of stability is much wider at higher voltages, such as approximately 2.3 volts where the range of stability is from -2.0v to +0.3v. Although the zener diode 300 configuration has several advantages including greater stability, less complex construction, etc., it still requires a greater operational voltage than may be desired in certain applications. Therefore, either the diode pair 110, 112 configuration or the zener diode 300 configuration may be used depending on the characteristics of the particular circuit within which the memory array 100 operates.

[0035] For purposes of this description, it will be assumed that the zener voltage  $V_z$  is approximately -2.0 volts. As described above, the initial voltage to which all columns and rows are set must be approximately equal. In this case, the initial voltage to which all columns (e.g., 104) and rows (e.g., 106) are set must be approximately  $V_z + V$  (e.g., approximately -2.2 volts). As depicted in Fig. 3(a), initially, column line 104 and row line 106 are charged to the same voltage, e.g.,  $V_z + 0.2v$  and therefore there is a voltage potential difference across memory cell 305 of approximately 0v and no current flows through programmable conductor memory element 114.

[0036] Turning to Fig. 3(b), a read operation is depicted whereby row line 106 is brought to ground, thereby introducing a large voltage potential difference across memory cell 305 and current begins to flow through the programmable conductor memory element 114. For example, when row line 106 is brought to zero volts a difference of potential of  $V_z$  (e.g., -2.0v) is registered across zener diode 300 leaving a voltage drop of approximately 0.2v across programmable conductor memory element 114. As described above, approximately 0.2v is sufficient to read the contents of the memory element 114; however, it is insufficient to program the memory element 114.

[0037] Fig. 6 depicts a flow chart of an operational flow for performing a read operation on a memory cell (e.g., 108), in accordance with exemplary embodiments of the invention. At segment 600, the process flow begins. At segment 605, all rows and columns are held to an initial voltage (e.g.,  $V_t + V$ , where  $V$  is a voltage suitable for reading

a memory element, but insufficient to program it; one exemplary  $V$  value as described above is 0.2 volts). The initial voltage may be introduced to all rows and columns via precharge circuits 116 and 118. This may be followed by equilibrating the voltages at the rows and columns. At segment 610, a reference voltage  $V_{ref}$  for a sense amplifier 102 connected to a selected column is set to approximately  $V_t + 0.1v$  (assuming  $V=0.2v$ ). At segment 615, a desired row is selected by bringing the row line 106 voltage to approximately zero volts (e.g., ground). At segment 620, current begins to flow in the selected memory cell associated with the row line, 106. At segment 625, the voltage on the column line, e.g., 104, of the desired cell 108 discharges from approximately  $V_t + V$  through the memory element 114 to the grounded row line. At segment 630, an N-sense amplifier portion (700 of Fig. 7) of sense amplifier 102 is enabled a predetermined time (e.g., 10-20 ns) after segment 615 brings the desired row line voltage to approximately zero volts. At segment 635, the resistance level of memory cell 108 is initially recognized by comparing the voltage at column line 104 with  $V_{ref}$  when the N-sense amplifier 700 is enabled. At segment 640, a determination is made as to whether column line 104 voltage had discharged below  $V_{ref}$ . If yes, at segment 650, the voltage at column line 104 is driven to approximately ground and a low resistance level is recognized at the programmable conductor memory element 114. If not, at segment 645, a high resistance level is recognized at the programmable conductor memory element 114.

[0038] At segment 655, a P-sense amplifier portion (800 of Fig. 8) of sense amplifier 102 is enabled a predetermined time (e.g., 10 ns) after the N-sense amplifier 700 is enabled at segment 630. At segment 660, if a high resistance level was recognized at segment 645, column line 104 is boosted to approximately  $V_{dd}$  and a logic HIGH state is read for the programmable conductor memory element 114. If a low resistance level was recognized at segment 650, a logic LOW state is read for the programmable conductor memory element 114.

[0039] If a low resistance level (e.g., logic LOW state) is read for the programmable conductor memory element 114 at segment 665, the row line 106 is boosted to

approximately  $V_{dd}$  so as to introduce a voltage potential across the programmable conductor memory element 114 sufficient to program the low resistance level back into the element. That is, by boosting the row line 106 voltage to  $V_{dd}$  while the voltage at the column line 104 is approximately grounded, a voltage sufficient to program the programmable conductor memory element 114 is introduced across the element 114. At segment 670, all column lines and all row lines are returned to the same initial voltage (e.g.,  $V_t + V$ ) for the next read cycle. The process flow ends at segment 675.

[0040] Turning to Fig. 7, an N-sense amplifier portion 700 of sense amplifier 102 (of Fig. 1) is depicted. N-sense amplifier 700 contains two inputs. A first input receives  $V_{ref}$ . A second input receives the voltage at column line 104. The first input (from  $V_{ref}$ ) is coupled to a first source/drain terminal of a complimentary metal oxide semiconductor (CMOS) transistor 702 and also coupled to a gate of CMOS 704. The second input of N-sense amplifier 700 is coupled to a source/drain terminal of CMOS 704 and a gate of CMOS 702. A second source/drain terminal of CMOS 702 is coupled to a second source/drain terminal of CMOS 704, and both in turn are coupled to a first source/drain terminal of CMOS 706. A gate of CMOS 706 receives a Fire N control signal, the receipt of which enables the N-sense amplifier 700 to determine whether the voltage of column line 104 is greater or less than  $V_{ref}$ . A second source/drain terminal of CMOS 706 is coupled to ground.

[0041] During operation of N-sense amplifier 700, if the voltage at column line 104 is greater than  $V_{ref}$ , then CMOS 704 is off and CMOS 702 is on and  $V_{ref}$  is driven to ground and the voltage at column line 104 remains floating while discharging from its initial level of  $V_t + V$ .

[0042] Alternatively, if the voltage at column line 104 is less than  $V_{ref}$ , then CMOS 704 is on and CMOS 702 is off, and the voltage at column line 104 is driven to ground and  $V_{ref}$  remains steady.

[0043] Turning now to Fig. 8, a P-sense amplifier portion 800 of sense amplifier 102 (of Fig. 1) is depicted. A first input of P-sense amplifier 800 receives Vref, and a second input receives the voltage at column line 104. A first source/drain terminal of CMOS 802 is coupled to Vref. A gate of CMOS 804 is also coupled to Vref. The voltage at column line 106 is coupled to a gate of CMOS 802 and also coupled to a first source/drain terminal of CMOS 804. A second source/drain terminal of CMOS 802 is coupled to a first source/drain terminal of CMOS 806 and a second source/drain terminal of CMOS 804 is also coupled to the same source/drain terminal of CMOS 806. A second source/drain terminal of CMOS 806 is coupled to a predetermined voltage level (e.g., Vdd). A gate of CMOS 806 receives a Fire P control signal, the receipt of which enables the P-sense amplifier 800 to further compare its input voltages.

[0044] During operation, the P-sense amplifier 800 is enabled a predetermined time after the N-sense amplifier 700 is enabled. That is, an initial determination has already been made as to whether the voltage at column line 104 is greater than or less than Vref and one of the voltages at column line 104 and Vref has been driven to ground. For example, if the voltage at column 104 was less than Vref for the input of N-sense amplifier 700, then the column line input to the N-sense amplifier 700 would have been driven to ground and would thus be considered a logic LOW for purposes of the input to P-sense amplifier 800. Vref would remain at its initial voltage. As a result, CMOS 804 would be inactive and CMOS 802 would be active, thus, increasing Vref to a predetermined voltage level (e.g., Vdd). If, however, as described above the voltage at column line 104 is greater than Vref, then Vref has been driven to ground and the column line input to the P-sense amplifier would be considered a logic HIGH and Vref would be considered a logic LOW. In this case, CMOS 802 would be off and CMOS 804 would be on and the voltage at column line 104 would be driven to the predetermined voltage (e.g., Vdd).

[0045] Turning now to Fig. 9, a timing diagram describing a read operation in accordance with an exemplary embodiment of the invention is described. Fig. 9 is a timing diagram for reading a high resistance value in the programmable conductor memory

element 114. Initially, all column lines and row lines of memory array 100 are at the same voltage (e.g.,  $V_t + 0.2v$ ). At time  $t_1$ , a selected row line (e.g., 106) is brought to zero volts and the voltage at column line 104 discharges through the programmable conductor memory element 114 of the selected memory cell 108. At time  $t_2$ , the N-sense amplifier 700 is enabled and a comparison is made between the voltage at column line 104 and the voltage on the Vref line 194. If, as depicted here, the voltage at column line 104 is greater than Vref, then Vref is driven to ground and the programmable conductor memory element 114 is recognized as having a high resistance value. At time  $t_3$ , the P-sense amplifier 800 is enabled and compares Vref with the voltage level at column line 104. As mentioned earlier, since Vref was driven to ground and the voltage of column line 104 is floating, voltage at column line 104 is driven to a predetermined voltage (e.g., Vdd) and a logic HIGH state is read for the element 114. Since the voltage at row line 106 remains at zero volts, a large enough voltage potential difference is seen across programmable conductor memory element 114 so as to enable a re-programming of its contents, if necessary. Subsequently, all row lines and column lines are brought to the same voltage value for a next read operation via precharge circuits 116 and 118. In addition, Vref is returned back to  $V_t + 0.1v$  from ground, where it was driven to by the N-sense amplifier 700. As described above in connection with Fig. 1, this may be achieved with Vref precharge circuit 192.

[0046] Turning to Fig. 10, a timing diagram for reading a low resistance value in programmable conductor memory element 114 is depicted. As in Fig. 9, and as described above, all columns and rows are initially at the same voltage (e.g.,  $V_t + 0.2v$ ) and at  $t_1$ , a selected row line (e.g., 106) is brought to zero volts. When the selected row line (e.g., 106) is brought to zero volts, a current flows through the programmable conductor memory element 114 of the selected memory cell 108 and the voltage of column line 104 discharges. At  $t_2$ , the N-sense amplifier 700 is enabled and compares the voltage at column line 104 with Vref. As depicted here, the voltage at column line 104 is lower than Vref (indicating that the programmable conductor memory element 114 contains a low

resistance level) and therefore column line 104 is driven to ground and Vref remains at  $V_t + 0.1v$ . At  $t_3$ , the P-sense amplifier is enabled and compares Vref ( $V_t + 0.1v$ ) with the voltage at column line 104 (now grounded). As a result, Vref is driven to a predetermined voltage, e.g., Vdd) and the voltage at column line 104 remains at ground. Here, the zero volts at column line 104 may be read as a logic "LOW" state.

[0047] The voltage at row line 106 is then raised to a predetermined voltage (e.g., Vdd) in order to enable a re-programming of the logic LOW state of the programmable conductor memory element 114. That is, by raising row line 106 to approximately Vdd, a sufficiently high voltage is seen across the programmable conductor element 114 so as to enable a programming operation. Subsequently, as described above, both the voltage at row line 106 and the voltage at column line 104 are brought to the same initial voltage (in fact, all column lines and all row lines of memory array 100 are brought to the same initial voltage), e.g.,  $V_t + 0.2v$ , for a next read operation via precharge circuits 116 and 118. Similarly, the Vref line 194 is returned back to e.g.,  $V_t + 0.1V$ . This may be achieved with Vref precharge circuit 192.

[0048] Fig. 11 illustrates a block diagram of a processor system 1100 containing a PCRAM semiconductor memory as described in connection with Figs. 1-10. For example, the PCRAM memory array 100 described in connection with Figs. 1-10 may be part of random access memory (RAM) 1108 and may be configured as one or more PCRAM memory circuits provided in a plug-in memory module. The processor-based system 1100 may be a computer system or any other processor system. The system 1100 includes a central processing unit (CPU) 1102, e.g., a microprocessor, that communicates with floppy disk drive 1112, CD ROM drive 1114, and RAM 1108 over a bus 1120. It must be noted that the bus 1120 may be a series of buses and bridges commonly used in a processor-based system, but, for convenience purposes only, the bus 1120 has been illustrated as a single bus. An input/output (I/O) device (e.g., monitor) 1104, 1106 may also be connected to the bus 1120, but is not required in order to practice the invention. The processor-based

system 1100 also includes a read-only memory (ROM) 1100 which may also be used to store a software program.

[0049] Although the Fig. 11 block diagram depicts only one CPU 1102, the Fig. 11 system could also be configured as a parallel processor machine for performing parallel processing. As known in the art, parallel processor machines can be classified as single instruction/multiple data (SIMD), meaning all processors execute the same instructions at the same time, or multiple instruction/multiple data (MIMD), meaning each processor executes different instructions.

[0050] The present invention provides a PCRAM cell 108 and a method for reading the logic state of a programmable conductor memory element 114 of the memory cell 108. According to an exemplary embodiment, the memory cell 108 consists of a first terminal of a programmable conductor memory element 114 coupled to a reverse connected diode pair 110, 112. Another terminal of the programmable conductor memory element 114 is coupled to a column line associated with the PCRAM cell 108. Another end of the reverse connected diode pair 110, 112 is coupled to a row line associated with the PCRAM cell 108.

[0051] Initially, all rows and columns of the memory array 100 are precharged to the same voltage potential (e.g.,  $V_t + V$ ). A row line is selected by bringing it to ground (e.g., approximately 0v).  $V$  is selected so that when  $V_t$  is across the diode pair 110, 112, a voltage sufficient to read the contents of the memory element 114, but insufficient to program the memory element 114, is across the memory element 114.

[0052] A predetermined time after a selected row line is brought to 0v and current begins to flow through the programmable conductor memory element 114, a comparison is made between the voltage of the column line (e.g., 104) and the reference voltage,  $V_{ref}$ . If the voltage at the column line is greater than  $V_{ref}$ , then  $V_{ref}$  is driven to ground and a high resistance level is recognized for the memory element 114. If the voltage at the column line is lower than  $V_{ref}$ , then the column line is driven to ground and a low

resistance level is recognized for the memory element 114. A predetermined time after such comparison is made, another comparison is made between the same two values and the contents of the programmable conductor memory element 114 are read.

[0053] For example, if  $V_{ref}$  was driven to ground, then the voltage at the column line 104 is driven to  $V_{dd}$  and e.g., a logic HIGH level is read for the programmable conductor memory element 114. If the column line was driven to ground, then  $V_{ref}$  is driven to  $V_{dd}$  and e.g., a logic LOW level is read for the programmable conductor memory element 114.

[0054] The voltage across the PCRAM cell 108 is then raised so as to increase the voltage potential difference across the memory element 114 to a level sufficient for programming (e.g., reprogramming a low resistance level for programmable conductor memory element 114 after a read operation).

[0055] While the invention has been described in detail in connection with preferred embodiments known at the time, it should be readily understood that the invention is not limited to the disclosed embodiments. Rather, the invention can be modified to incorporate any number of variations, alterations, substitutions or equivalent arrangements not heretofore described, but which are commensurate with the spirit and scope of the invention. For example, although the invention has been described in connection with specific voltage levels, it should be readily apparent that any other voltage levels can be selected to achieve the same results. In addition, although the invention has been described in connection with specifically placed n-type and p-type CMOS transistors, it should be readily apparent that the inverse of these CMOS transistors can be used instead. Furthermore, although the invention is described in connection with a reverse connected diode pair 110, 112 coupled between the programmable conductor memory element 114 and the row line 106, the reverse connected diode pair 110, 112 can be moved to a location between the programmable conductor memory element 114 and the column line 104. In addition, although an exemplary embodiment of the invention depicts the zener

diode 300 with a certain orientation in the circuit, that orientation may be reversed and the location of the zener diode moved to the other side of the programmable conductor memory element 114.

[0056] Furthermore, although the invention is described as reducing the voltage at a selected row line to approximately zero volts, it may be the column line that is reduced to approximately zero volts. In the alternative, either one of the row low or column line may be increased to create a voltage potential difference across selected memory cell 108. Accordingly, the invention is not limited by the foregoing description or drawings, but is only limited by the scope of the appended claims.